

Lead Engineer - JD(DJD2021032)



Roles	Lead Engineer - FPGA Design
Responsibilities	<ul style="list-style-type: none"> • Meeting with design and engineering teams to determine FPGA requirements. • The role involves contributing to the entire FPGA based product development flow starting from requirement analysis till final product testing in lab environment. • The candidate will be responsible for architecture/micro-architecture design and implementation of the logic in VHDL for targeted FPGA, writing test benches to validate the design etc. • Troubleshooting and diagnosing errors and suggesting suitable repairs or modifications • Job involves frequent interaction with board design, software, testing and lab teams to deliver the product meeting the customer requirements. • Work closely with cross-functional team to achieve assigned project/activity targets within boundaries of Time, Cost and Quality • Conducting the internal/External design reviews to ensure adherence to the company design process. • Technical guidance to the junior engineers
Category	Description
Qualifications	BE/ in Electronics, Specialisation in VLSI and Embedded Design is a plus
Experience	6 to 9 years experience designing and implementing FPGA based solution in Xilinx or Altera FPGA, preferably FPGA based product development experience, executing projects in Defence / Industrial , Rail , Healthcare, Retail Automation, etc. in Electronic Domain
	<ul style="list-style-type: none"> • Generation of FPGA requirements document and FPGA design documents • Design architecture for FPGA based solutions. • VHDL, Verilog based RTL design and Development • VHDL, Verilog based Verification and Validation, Testbench creations . • Knowledge of Xilinx ISE, Vivado, Intel/Altera Quartus & Lattice diamond tools.

Technical & Process Capabilities	<ul style="list-style-type: none"> • Should have worked on PCIe, DDR4, DDR3, Video protocols (HD,SD & Parallel Video processing), ADC, DAC, USB & Ethernet based design experience. • Should have worked on UART, I2C, SPI & Parallel memory interface designs. • Should have knowledge on CLOCK DOMAIN CROSSING DESIGN, STA (Static Timing Analysis) & Debug techniques. • experience in board level testing and system debugging • Should have strong problem solving and debugging skills
Behavioural	Collaborative , Capable to interact / interface with customers, cross functional team
	Self driven
	Excellent Communicaiton, verbal & written
	Passionate & Learning ability
Values	Accountable & Responsible
	Ethics & Integrity, Knowledge, Collaboration, Caring, Agility, Empowerment with Accountability and Sustainability
Preferred Experience, Knowledge & Attributes	Defence, Industrial , Allied domain Knowledge
	Solution / system engg capabilities
Compensation	To be filled by HR

